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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,608	12/24/2003	CHIH-FENG SUNG	10217-US-PA	1607

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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER
TRAN, THUY V

ART UNIT	PAPER NUMBER
2821	

NOTIFICATION DATE	DELIVERY MODE
09/05/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USA@JCIPGROUP.COM.TW

Office Action Summary	Application No.	Applicant(s)	
	10/707,608	CHIH-FENG SUNG	
	Examiner	Art Unit	
	Thuy V. Tran	2821	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *RCE filed on 08/13/2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-17 and 21-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-17 and 21-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is responsive to the Applicant's Request for Continued Examination (RCE) filed on 08/13/2007 and preliminary amendment concurrently filed therewith. In virtue of this amendment:

- Claims 1-11 and 18-20 have been canceled; and thus,
- Claims 12-17 and 21-24 are now presented in the instant application.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 12-17 and 21-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Asano et al. (Pub. No.: US 2002/0190924 A1; hereinafter "Asano").

With respect to claim 12, Asano discloses, in Fig. 1, an organic light-emitting display comprising (1) a pixel array having a plurality of data lines [Y(i), Y(i+1), Y(i+2)]], a plurality of scan lines [X(i), X(i+1), X(i+2)], and a plurality of first and second pixels (whether pixels in row as the first and in column as the second, or vice-versa; see Fig.1), wherein each of the first and second pixels is electrically connected to one of the scan lines and one of the data lines correspondingly (see pixel [i, i] with connections to the scan line X(i) and the data line [Y(i)]), (2) a first external power line (which is connected to line [14] and to pixels in the first column shown in Fig. 1), dividing into a plurality of first internal power lines (connected to EL of each

pixel; see Fig. 1), wherein each first internal power line is electrically connected to at least two of the first pixels (see Fig. 1), (3) a second external power line (which is connected to line [14] and to each pixels on the second column shown in Fig. 1), dividing into a plurality of second internal power lines (connected to EL of each pixel; see Fig. 1), wherein each second internal power line is electrically connected to at least two of the second pixels, and the first internal power lines and the second internal power lines are separated (see Fig. 1), and (4) a power source [Vo] electrically connected to the first and second external power lines (see Fig. 1), wherein the first external power line and the second external power line provide a same power signal (from power source [Vo]; see Fig. 1) to the first pixels and the second pixels.

With respect to claim 13, Asano discloses, in Fig. 1, that each of the first and second pixels comprises (i) a switching transistor [TRiia] having a first drain electrode, a first gate electrode, and a first source electrode, wherein the first drain electrode is coupled to one of the data lines [Yi, Y(i+1), Y(i+2)], and the first gate electrode is coupled to one of the scan lines [Xi, X(i+1), X(i+2)], (ii) a driving transistor [TRiib] having a second drain electrode, a second gate electrode, and a second source electrode, wherein the second gate electrode is coupled to the first source electrode, and the second source electrode is grounded (connected to the common ground line [15]; see Fig. 1), (iii) a storage capacitor [Cii], having a first terminal and a second terminal, wherein the first terminal is coupled to the first source electrode and the second gate electrode, and the second terminal is grounded (connected to the common ground line [15]; see Fig. 1) and coupled to the second source electrode, and (iv) a light-emitting device [ELii], having an anode and a cathode, wherein the anode is coupled to one of the first and second internal power lines (see Fig. 1) and the cathode is coupled to the second drain electrode.

With respect to claim 14, Asano discloses, in Fig. 1, that the switching transistor [TRiia] comprises a thin film transistor (see paragraph [0030], lines 1-2).

With respect to claim 15, Asano discloses, in Fig. 1, that the driving transistor [TRiib] comprises a thin film transistor (see paragraph [0030], lines 1-2).

With respect to claim 16, Asano discloses, in Fig. 1, that the light-emitting device comprises an organic light-emitting diode [ELii] (see paragraph [0026], line 1).

With respect to claim 17, Asano discloses, in Fig. 2, that the light-emitting device [Elii] comprises a polymer light-emitting diode (since it contains a transparent conductive layer, at least, which is inherently made of polymer (transparent layer)).

With respect to claim 21, Asano discloses, in Fig. 1, an organic light-emitting display comprising (1) a pixel array having a plurality of data lines [Y(i), Y(i+1), Y(i+2)], a plurality of scan lines [X(i), X(i+1), X(i+2)] and a plurality of first and second pixels arranged in a matrix of columns and rows (see Fig. 1), wherein each of the first and second pixels is electrically connected to one of the scan lines and one of the data lines correspondingly, (2) a first external power line (which is connected to line [14] and to pixels in the first column shown in Fig. 1), dividing into a plurality of first internal power lines (connections to it within the pixels; see Fig. 1), wherein each first internal power lines is electrically connected to the first pixels in the same column or in the same row, (3) a second external power line (which is connected to line [14] and to pixels in the second column shown in Fig. 1), dividing into a plurality of second internal power lines (connected to EL of each pixel in the second column; see Fig. 1), wherein each second internal power lines is electrically connected to the second pixels in the same column or in the same row, wherein the first internal power lines and the second internal power lines are

separated (see Fig. 1), and (4) a power source [Vo] electrically connected to the first and second external power lines, wherein the first external power line and the second external power line provide a same power signal (from power source [Vo]; see Fig. 1) to the first pixels and the second pixels.

With respect to claim 22, Asano discloses, in Fig. 1, that that each of the first and second pixels comprises (i) a switching transistor [TRiia] having a first drain electrode, a first gate electrode, and a first source electrode, wherein the first drain electrode is coupled to one of the data lines [Yi, Y(i+1), Y(i+2)], and the first gate electrode is coupled to one of the scan lines [Xi, X(i+1), X(i+2)], (ii) a driving transistor [TRiib] having a second drain electrode, a second gate electrode, and a second source electrode, wherein the second gate electrode is coupled to the first source electrode, and the second source electrode is grounded (connected to the common ground line [15]; see Fig. 1), (iii) a storage capacitor [Cii], having a first terminal and a second terminal, wherein the first terminal is coupled to the first source electrode and the second gate electrode, and the second terminal is grounded (connected to the common ground line [15]; see Fig. 1) and coupled to the second source electrode, and (iv) a light-emitting device [ELii], having an anode and a cathode, wherein the anode is coupled to one of the first and second internal power lines (see Fig. 1) and the cathode is coupled to the second drain electrode.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asano et al. (Pub. No.: US 2002/0190924 A1; hereinafter "Asano").

With respect to claims 23-24, Asano discloses all of the claimed limitations, as expressly recited in claims 12 and 21, except that the first and second external power lines are disposed at two opposite sides of the pixel array. However, this difference is not of patentable merits since it is believed that such an arrangement does not affect the operation capability of the display device. Specifically, in either opposite or same side position, the operation of the display is still the same, since these two external power lines are neither connected to the signal/data lines nor the scanning lines. Therefore, to configure the two external power lines at two opposite sides of the pixel array for convenience in relocating the related components/parts of the display would have been deemed obvious to a person skilled in the art.

Remarks and conclusion

5. Applicant's arguments with respect to amended claims 12 and 21 filed on 08/13/2007 have been fully considered but they are not persuasive.

In response to Applicant's argument in the second paragraph at page 9 that "a power source electrically connected to the first and second external power lines, wherein the first external power line and the second external power line provide a same power signal to the first pixels and the second pixels", it is noted that Asano apparently discloses such features. Specifically, Asano discloses in Fig. 1 that the power source [Vo] is electrically connected to the first and second external power lines (which are directly connected to line [14] and to [EL] in each pixel), and that the first external power line and the second external power line provide a

same power signal (provided by [Vo]) to the first pixels (in the first column) and the second pixels (in the second column).

Therefore, claims 12-17 and 21-22 remain rejected under 35 U.S.C. 102(e) as being anticipated by Asano (see "Claim Rejections – 35 USC § 102" set forth above for details), and claims 23-24 are rejected as being unpatentable over the teaching of Asano (see "Claim Rejections – 35 USC § 103" set forth above for details).

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thuy V. Tran whose telephone number is (571) 272-1828. The examiner can normally be reached on M-F (8:00 AM -4:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Owens Douglas can be reached on (571) 272-1662. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

08/29/2007

THUY V. TRAN
PRIMARY EXAMINER